

AT91SAM7A3-EK Evaluation Board

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User Guide



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Section 1

Overview

-
- 1.1 Scope** The AT91SAM7A3-EK evaluation kit enables evaluation capabilities and code development of applications running on an AT91SAM7A3.
- This guide focuses on the AT91SAM7A3-EK board as an evaluation platform.
-
- 1.2 Deliverables** The AT91SAM7A3-EK package contains the following items:
- an AT91SAM7A3-EK board
 - one A/B-type USB cable
 - one serial RS232 cable
 - one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM[®] Thumb[®] 32-bit microcontroller quickly.
-
- 1.3 The AT91SAM7A3-EK Evaluation Board** The board is equipped with an AT91SAM7A3 (100-pin LQFP Green package) together with the following:
- USB device port interface
 - one DBGU serial communication port
 - JTAG/ICE debug interface connector
 - two serial CAN communication ports
 - one serial LIN communication port
 - one buffered analog input and PWM output
 - one Power LED and four general-purpose LEDs
 - one SD/MMC/DataFlash[®] card slot
 - expansion connector
 - one Atmel[®] serial DataFlash
 - one footprint for 3.6V lithium thionyl-chloride backup battery





Section 2

Setting Up the AT91SAM7A3-EK Evaluation Board

2.1 Electrostatic Warning The AT91SAM7A3-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements In order to set up the AT91SAM7A3-EK evaluation board, the following items are required:

- the AT91SAM7A3-EK evaluation board itself
- an A/B-type USB cable

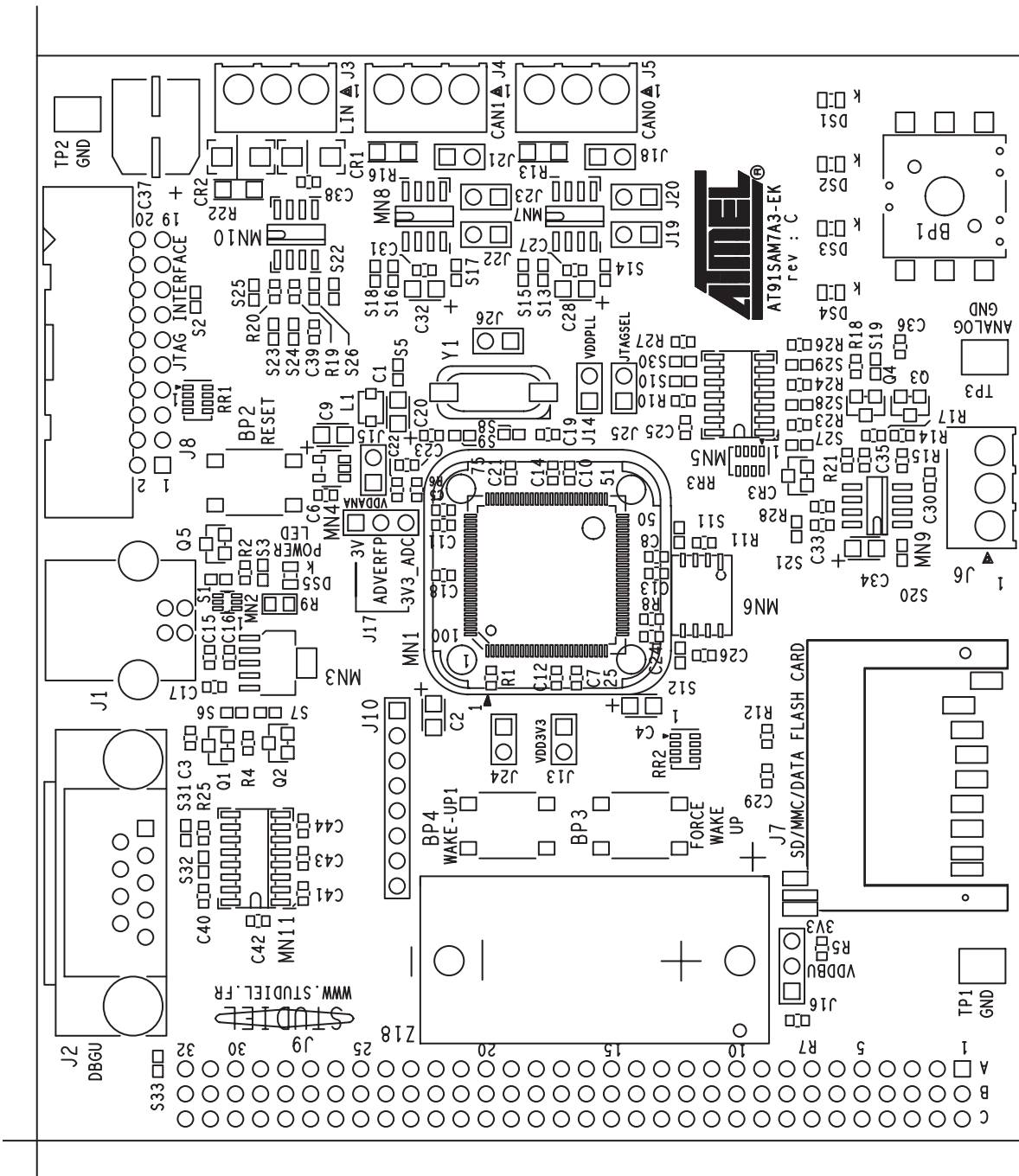
or

- a DC USB power adapter (5V at 0.5 A) with USB A/B cable

Note: The AT91SAM7A3-EK is not delivered with a JTAG/ICE interface which is required to start evaluating the device.

2.3 Layout

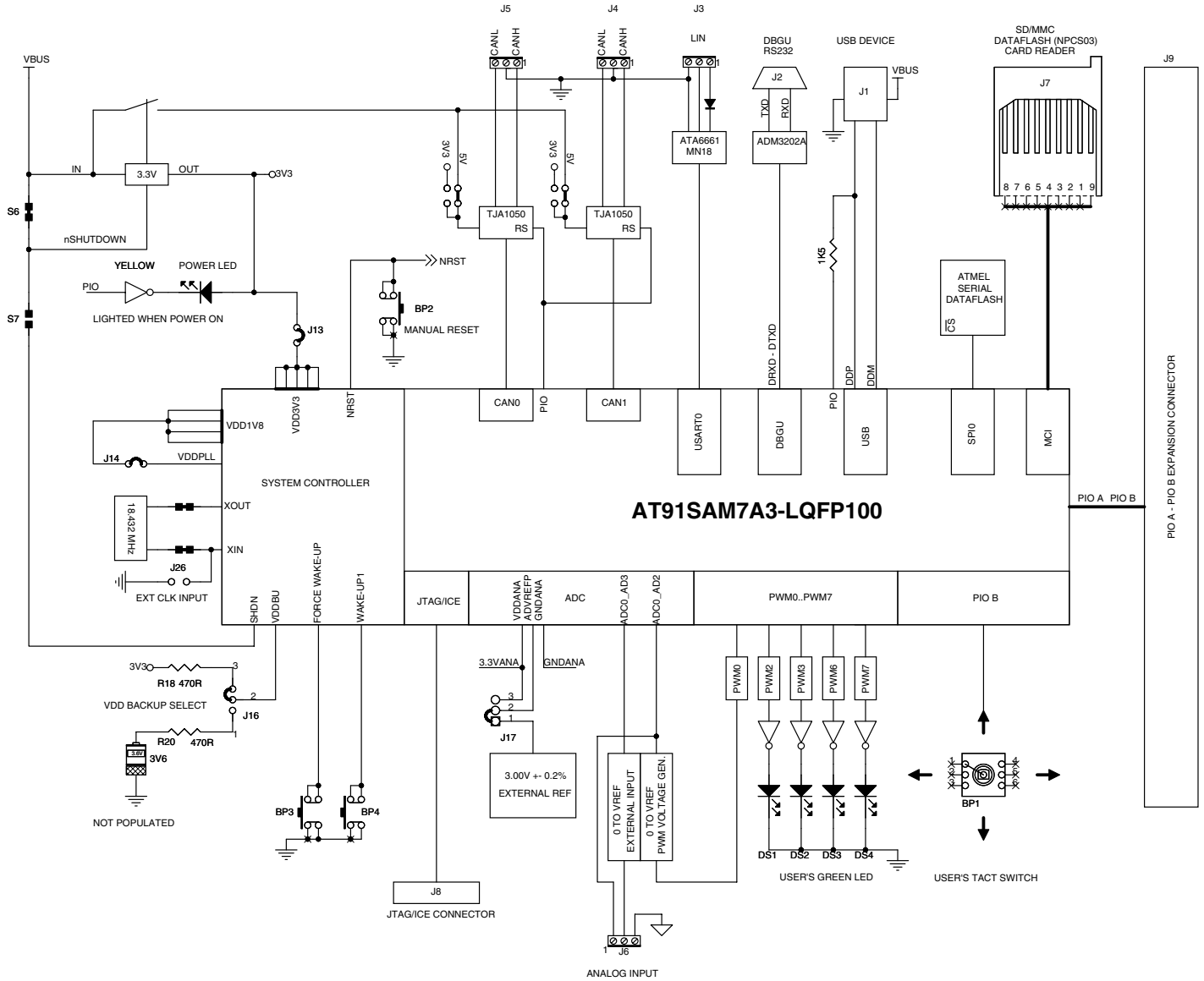
Figure 2-1. Top Level Layout



-
- 2.4 Powering Up the Board** AT91SAM7A3 is self-powered by the USB port or by a USB power adapter.
-
- 2.5 Backup Power Supply** The user may add a battery (SAFT LS14250 3.6V or equivalent) in order to permanently power the backup part of the device. In this case, the configuration of J16, S6 and S7 must be changed.
Refer to [Table 4-1](#).
-
- 2.6 Getting Started** The AT91SAM7A3-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the Atmel web site, <http://www.atmel.com/products/AT91/>, for the most up-to-date information on getting started with the AT91SAM7A3-EK.
- Note that the AT91SAM7A3 microcontroller fitted on the evaluation board has been programmed with the SAM Boot Assistant (SAM-BA™) which provides an easy way to program the embedded Flash memory through the USB or DBGU communication channel.
- Programming through DBGU requires that the evaluation kit is powered using a Power Supply USB Adapter
- Note:** The SAM-BA Boot Assistant resides in the embedded Flash memory and will be deleted when programming the Flash. A JTAG/ICE interface is required to recover SAM-BA Boot Assistant.

2.7 AT91SAM7A3-EK Block Diagram

Figure 2-2. Block Diagram





Section 3

Board Description

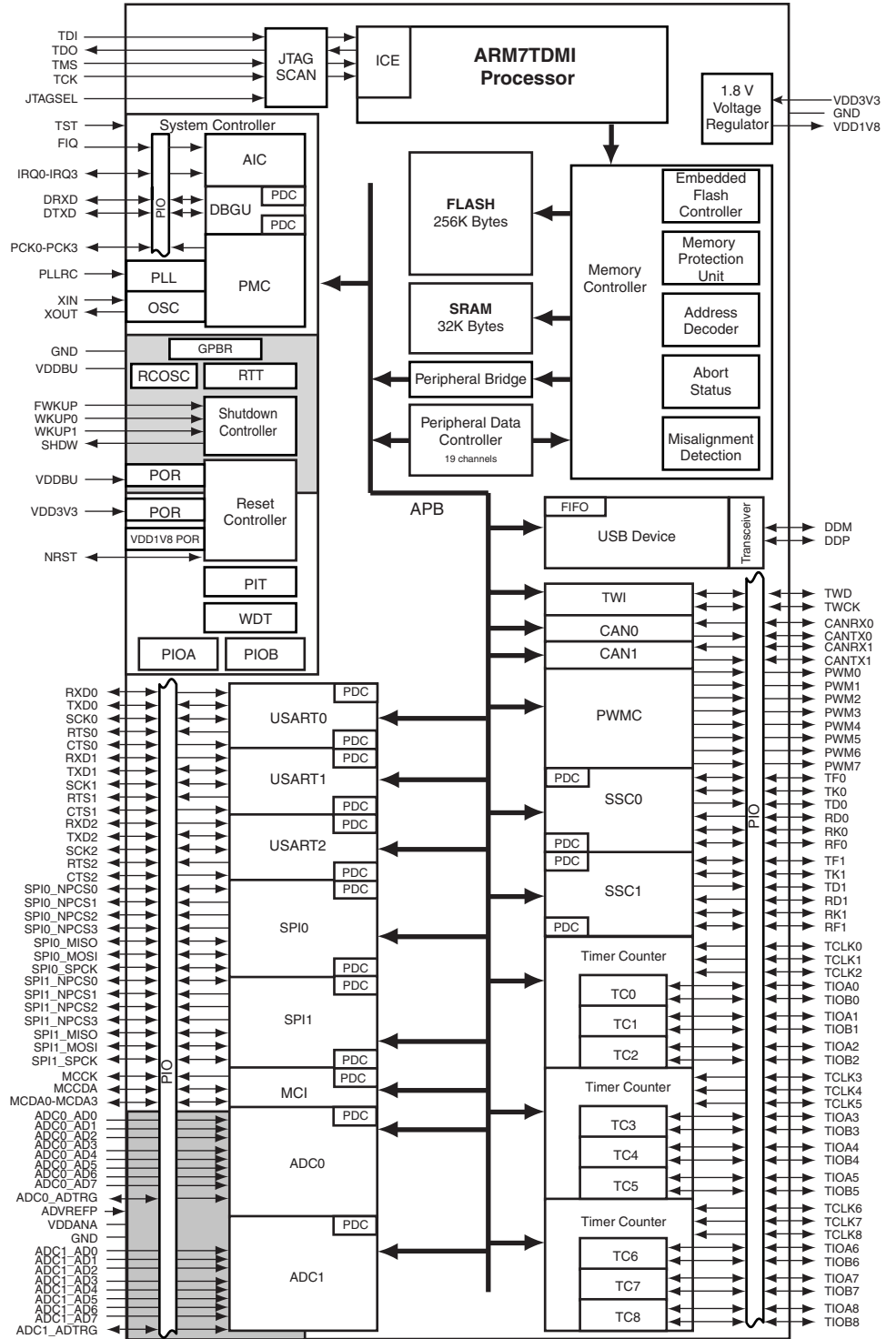
- 3.1 AT91SAM7A3 Microcontroller**
- Incorporates the ARM7TDMI[®] ARM[®] Thumb[®] Processor
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - Embedded ICE In-circuit Emulation, Debug Communication Channel Support
 - 256 Kbytes of Internal High-speed Flash, Organized in 1024 Pages of 256 Bytes
 - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
 - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
 - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
 - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities
 - 32K Bytes of Internal High-speed SRAM, Single-cycle Access at Maximum Speed
 - Memory Controller (MC)
 - Embedded Flash Controller, Abort Status and Misalignment Detection
 - Memory Protection Unit
 - Reset Controller (RSTC)
 - Based on Three Power-on Reset Cells
 - Provides External Reset Signal Shaping and Reset Sources Status
 - Clock Generator (CKGR)
 - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and One PLL
 - Power Management Controller (PMC)
 - Power Optimization Capabilities, including Slow Clock Mode (Down to 500 Hz), Idle Mode, Standby Mode and Backup Mode
 - Four Programmable External Clock Signals
 - Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources

- Four External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
 - 2-wire UART and Support for Debug Communication Channel interrupt
- Periodic Interval Timer (PIT)
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signal to the System
 - Counter May Be Stopped While the Processor is in Debug Mode or in Idle State
- Real-time Timer (RTT)
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- Two Parallel Input/Output Controllers (PIO)
 - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Shutdown Controller (SHDWC)
 - Programmable Shutdown Pin and Wake-up Circuitry
- Two 32-bit Battery Backup Registers for a Total of 8 Bytes
- One 8-channel 20-bit PWM Controller (PMWC)
- One USB 2.0 Full Speed (12 Mbits per Second) Device Port
 - On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
- Nineteen Peripheral Data Controller (PDC) Channels
- Two CAN 2.0B Active Controllers, Supporting 11-bit Standard and 29-bit Extended Identifiers
 - 16 Fully Programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two 8-channel 10-bit Analog-to-Digital Converter
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interfaces (SPI)
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- Three 3-channel 16-bit Timer/Counters (TC)
 - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability

- Two Synchronous Serial Controllers (SSC)
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One Two-wire Interface (TWI)
 - Master Mode Support Only, All Two-wire Atmel EEPROMs Supported
- Multimedia Card Interface (MCI)
 - Compliant with Multimedia Cards and SD Cards
 - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- IEEE[®] 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
 - Embedded 1.8V Regulator, Drawing up to 130 mA for the Core and the External Components, Enables 3.3V Single Supply Mode
 - 3.3V VDD3V3 Regulator, I/O Lines and Flash Power Supply
 - 1.8V VDD1V8 Output of the Voltage Regulator and Core Power Supply
 - 3V to 3.6V VDDANA ADC Power Supply
 - 3V to 3.6V VDDBU Backup Power Supply
- 5V-tolerant I/Os
- Fully Static Operation: 0 Hz to 60 MHz at 1.65V and 85°C Worst Case Conditions
- Available in a 100-lead LQFP Green Package

3.2 AT91SAM7A3 Block Diagram

Figure 3-1. Block Diagram



-
- 3.3 Memory**
- 256 Kbytes of Internal High-speed Flash
 - 32 Kbytes of Internal High-speed SRAM
 - Atmel serial DataFlash
-
- 3.4 Clock Circuitry**
- 18.432 MHz standard crystal for the embedded oscillator
 - 32 KHz internal RC oscillator
-
- 3.5 Reset Circuitry**
- Internal reset controller with a bi-directional reset pin
 - External reset pushbutton
-
- 3.6 Shutdown Controller**
- Programmable shutdown and Wake-Up
 - Force Wake-Up and Wake-up pushbutton
-
- 3.7 Power Supply Circuitry**
- USB powered, the dynamic power consumption on VDD1V8 is less than 50 mA at full speed when running out of the Flash. The total current at power-up is less than 100 mA.
 - External power can be applied via USB Power adapter 5V 0.5A with USB A/B cable
 - On-chip embedded VDDCORE 1.8V regulator
 - On-board 3.3V linear regulator with shutdown control
-
- 3.8 Remote Communication**
- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
 - USB V2.0 Full-speed compliant, 12 Mbits per second (UDP)
 - Two CAN 2.0B communication ports via the 3-position printed circuit terminal block
 - One LIN communication port via the 3-position printed circuit terminal block
-
- 3.9 Analog Interface**
- One selectable 0.2% 3.00V Vref or 3.3V ANA
 - One 3-position printed circuit terminal block
 - Two analog up to Vref inputs. One external user input and one back-looped with buffered PWM0 output.
 - One buffered PWM0 analog output (up to Vref)
-
- 3.10 User Interface**
- One 5-way joystick (4 directions and push for confirmation)
 - Four general-purpose buffered green LEDs (PWM controlled)

- One yellow power LED (can also be software controlled)

-
- 3.11 Debug Interface**
- 20-pin JTAG/ICE interface connector
 - DBGU serial RS232 COM Port

-
- 3.12 Expansion Slot**
- One SD/MMC/DataFlash card slot
 - All I/Os of the AT91SAM7A3 are routed to peripheral extension connectors (J9). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.



Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J13	Closed	VDD3V3 Jumper ⁽¹⁾
J14	Closed	VDDPLL Jumper ⁽¹⁾
J15	Closed	VDDANA Jumper ⁽¹⁾
J16	2-3	VDDBU Jumper select ⁽¹⁾ 1-2 : Optional Lithium Thionyl Chloride 3.6V Backup Battery 2-3 : 3.3V power
J17	1-2	ADVREFP Jumper select ⁽¹⁾ 1-2 : 3.00V Voltage reference 2-3 : VDDANA
J18	Closed	Enables 120 ohms CAN bus resistance termination (CAN0)
J19	Closed	Enables 5V power supply for TJA1050 Transceiver. It is closed by wire on solder side. J19 and J20 should not be closed at the same time.
J20	Open	Disables 3.3V power supply for TJA1050 Transceiver. J20 and J19 should not be closed at the same time.
J21	Closed	Enables 120 ohms CAN bus resistance termination (CAN1)
J22	Closed	Enables 5V power supply for TJA1050 Transceiver. It is closed by wire on solder side. J22 and J23 should not be closed at the same time.
J23	Opened	Disables 3.3V power supply for TJA1050 Transceiver. J23 and J22 should not be closed at the same time.
J24	Opened	Do not use: Factory test mode
J25	Opened	Select ICE mode or JTAG mode (Closed)
J26	Opened	External XIN clock input. S8 and S9 must be open.

Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
S1	Opened	Solder it, enables permanent pull up on USB DP. S3 must be open.
S2	Closed	The System Reset signal (NRST) is connected to the ICE/JTAG socket (J8, pin 15).
S3	Closed	Enables the use of the USB DP PUP (PB1)
S4	Closed	Enables the use of the USB CNX detection (PB0)
S5	Closed	Digital Analog GND planes separation. Do not cut it
S6	Closed	Disables shutdown control and forces Power on. Do not close at same time as S7.
	Opened	Enables shutdown control
S7	Opened	Disables shut down control
	Closed	Enables shutdown control Do not close at same time as S6.
S8 - S9	Closed	Enables the use of 18.432 MHz crystal. Must be open if external clock used.
S10	Closed	Enables the Power LED control
S11	Closed	Enables the use of the NPCS13
S12	Opened	Disable Serial DataFlash write protect
S13	Closed	Enables the use of the TXD CAN0 transceiver (PA27)
S14	Closed	Enables the use of the RXD CAN0 transceiver (PA26)
S15	Closed	Enables control of the Standby/Normal mode for CAN0 and CAN1 transceivers (PA23)
S16	Closed	Enables the use of the TXD CAN1 transceiver (PA29)
S17	Closed	Enables the use of the RXD CAN1 transceiver (PA28)
S18	Opened	Enables control of the Standby/Normal mode for CAN0 and CAN1 transceivers (PA23). If S18 is closed, S15 must be open.
S19	Closed	Enables the use of PWM0 Analog Output (PA18)
S20	Closed	Enables the use of AD02 Analog Input (PB16)
S21	Closed	Enables the use of AD03 Analog Input (PB17)
S22	Closed	Enables the use of the TXD LIN transceiver (PA3)
S23	Closed	Enables the use of the RXD LIN transceiver (PA2)
S24	Closed	Enables the control of the EN LIN transceiver (PA5)
S25	Closed	Enables the control of the INH LIN transceiver (PA6)
S26	Opened	Do not use
S27	Closed	Enables the use of the User LED DS4 (PA25)
S28	Closed	Enables the use of the User LED DS3 (PA24)
S29	Closed	Enables the use of the User LED DS2 (PA21)
S30	Closed	Enables the use of the User LED DS1 (PA20)



Table 4-1. Configuration Jumpers and Straps (Continued)

Designation	Default Setting	Feature
S31	Closed	Enables the use of the DBGU TXD signal (PA31)
S32	Closed	Enables the use of the DBGU RXD signal (PA30)
S33	Opened	Disable VUSB power supply on J9 extension connector.
TP1	N.A	GND Test point
TP2	N.A	GND Test point
TP3	N.A	GND_ADC Test point

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

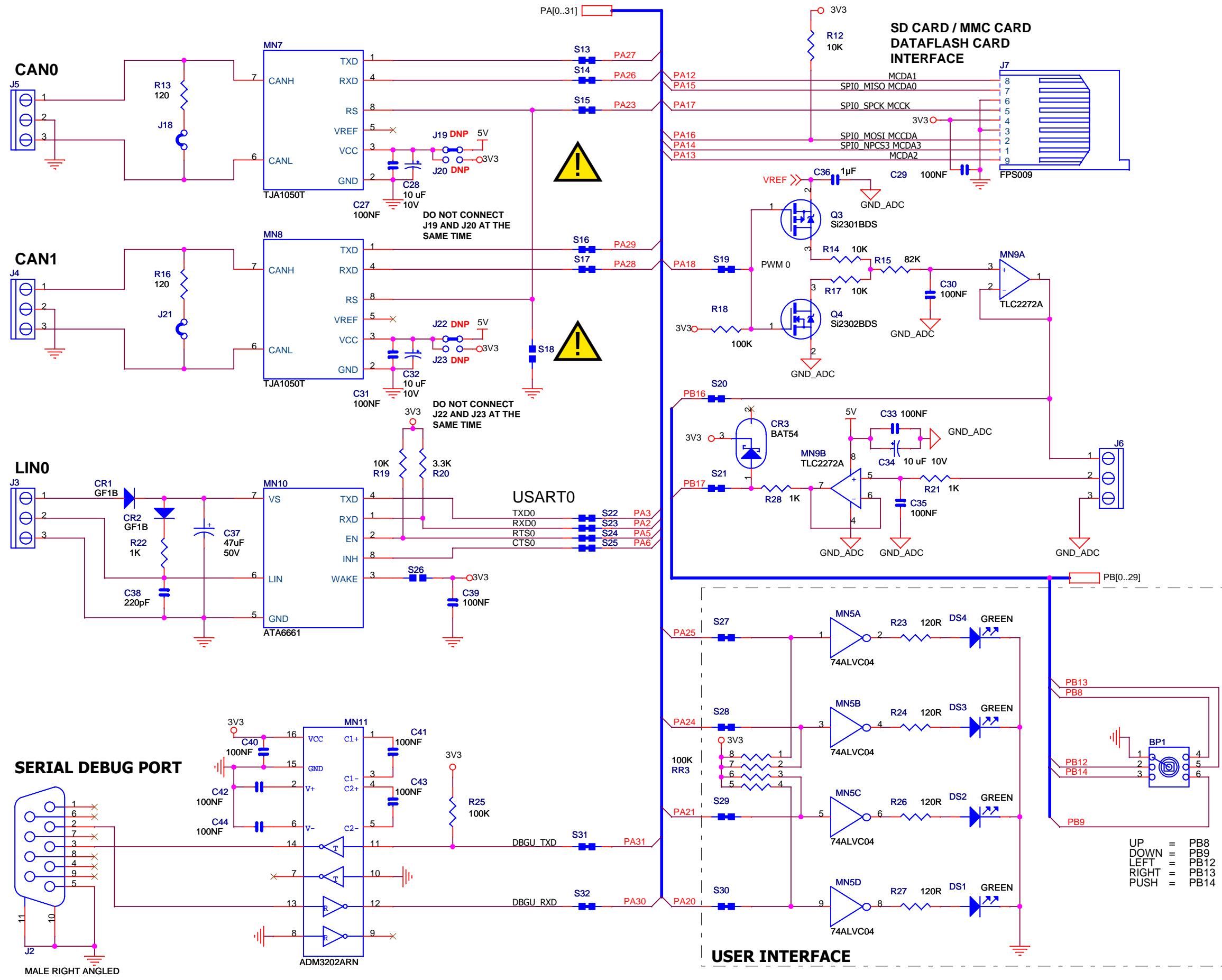




Section 5

Schematics

-
- 5.1 Schematics** This section contains the following schematics:
- Processor
 - I/O



Friday, June 09, 2006

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Section 6

Revision History

6.1 Revision History

Table 6-1.

Document	Comments	Change Request Ref.
6165A	First issue.	
6165B	Added information on SAM-BA in Section 2.6 .	05-415
6165C	Removed references to 32 Mbit serial DataFlash (AT45DB321C-CNC) in Section 1.3 and in Section 3.3 . Inserted new Figure 2-2 and new schematics in Section 5 .	2846





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